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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/970,388	10/02/2001	Seong-Hoon Lee	00939H-079810US	1994

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EXAMINER	
DINH, SON T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/970,388	LEE, SEONG-HOON	
	Examiner	Art Unit	
	Son T. Dinh	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *32-37* is/are allowed.

6)☒ Claim(s) *11-15,20-25,30,31,38 and 39* is/are rejected.

7)☒ Claim(s) *16-19,26-29 and 40-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/703,405.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/2/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *East search history*.

DETAILED ACTION

The pre-amendment filed on 10/2/01 has been entered.

Claims 1-10 have been canceled.

Claims 11-42 are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 11-15, 20-25, 30-31 and 38-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Harrison (U.S. Patent No 5,926,047).

Regarding claims 11 and 22, figure 3 of Harrison discloses a DLL comprising a digital locking circuit (68, 70, 66 and 67) for receiving an external clock signal (CCLKREF) and generating a DLL clock signal (the output of 67), wherein the DLL clock

signal is a delayed version of the external clock signal (performed by 68 and as shown in figure 3), an analog locking circuit (44, 40, 70) configured to receive the DLL clock signal (the output signal of 67 is applied to the element 44) from the digital clocking circuit (68, 54, 66 and 67) and check delayed version of the DLL clock signal against the external clock (CCLKREF) to generate a feedback signal that is fed back to the digital clocking circuit (66, 54, 66 and 67).

Regarding claims 12 and 23, the output signal of element 67 would be considered as a feedback signal and is used by the digital clocking circuit (66, 68, 70 and 67) to adjust the DLL clocking signal (the output signal of 67).

Regarding claims 13 and 24, the phase detector 54 would perform the function of checking the delayed version of the DLL clock signal against the external clock signal (CCLKREF) by detecting a phase difference between the delayed version (the output signal at 180 of 40) and the external clock signal (the output signal at TO of 40).

Regarding claims 15, 21, 25 and 31, figure 7 and claim 1 of Harrison clearly show that his DLL circuit is used in a memory device so as to allow the output data signal to be in synchronized with the external clock.

Regarding claims 20, 30, column 1, lines 2-23 discloses that the memory device is a synchronous DRAM.

Regarding claim 38, the step of generating an output clock signal by delaying the external clock signal is performed by element 68 (figure 3), the step of generating a comparison clock signal by delaying the output clock signal is performed by element 66 (figure 3), the step of comparing a phase difference between the comparison clock and

the output clock signal to form a feedback is performed by element 54 (figure 3) and the step of using the feedback signal to adjust the output clock signal is performed by element 62 (figure 3).

Regarding claim 39, Harrison clearly discloses that his circuit is used in a memory device for allowing the output data signal being synchronized with the external clock signal (see figure 7 and column 1, lines 20-23).

Allowable Subject Matter

Claims 16-19, 26-29 and 40-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 32-37 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fail to teach or suggest a particular structure of the digital locking circuit having particular connection between a first delay, a control circuit, a first voltage controlled oscillation circuit and a second voltage controlled oscillation circuit as claimed in claim 16, 26 and 32 and a method of operating such digital locking circuit as claimed in claim 40.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

-Leonowich disclose a DLL having a delay circuit.

-Hjerpe et al disclose a phase locked loop having a phase detector.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son T. Dinh whose telephone number is 571-272-1868. The examiner can normally be reached on Monday to Friday 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

S. Dinh
September 12, 2006

Son T. Dinh
Primary Examiner